EXPRESS MAIL NO.: EL872040006US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Brent Keeth	Attorney Docket No.: 500426.02
Filed	: Concurrently herewith	
Title	: METHOD AND APPARATUS FOR DATA COMPRESSION IN MEMORY DEVICES	

INFORMATION DISCLOSURE STATEMENT

Box Patent Application
Commissioner of Patents
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 09/139,838, filed August 25, 1998. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP

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Enclosure:
Form PTO-1449

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FORM PTO-1449 (REV.7-80)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.
500426.02	Not yet assigned
APPLICANT(S)	
Brent Keeth	
FILING DATE	GROUP ART UNIT
Concurrently herewith	Not yet assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,991,139	2/5/91	Takahashi et al.	365	201	
	AB	5,029,330	7/2/91	Kajigaya	365	201	
	AC	5,179,537	1/12/93	Matsumoto	365	201	
	AD	5,268,639	12/7/93	Gasbarro et al.	324	158 R	
	AE	5,289,415	2/22/94	DiMarco et al.	365	190	
	AF	5,305,272	4/19/94	Matsuo et al.	365	208	
	AG	5,451,898	9/19/95	Johnson	327	563	
	AH	5,488,321	1/30/96	Johnson	327	66	
	AI	5,519,661	5/21/96	Miura	365	205	
	AJ	5,621,340	4/15/97	Lee et al.	327	65	
	AK	5,684,750	11/4/97	Kondoh et al.	365	205	
	AL	5,708,607	1/13/98	Lee et al.	365	189.05	
	AM	5,809,038	9/15/98	Martin	371	21.2	
	AN	5,923,594	7/13/99	Voshell	365	189.05	
	AO	5,935,263	08/10/99	Keeth et al.	714	718	
	AP	5,953,266	9/14/99	Shore	365	200	
	AQ	5,959,921	09/28/99	Manning et al.	365	208	
	AR	6,005,816	12/21/99	Manning et al.	365	208	
	AS	6,032,274	02/29/00	Manning	714	718	
	AT	6,043,562	3/28/00	Keeth	257	776	
	AU	6,055,654	04/25/00	Martin	714	719	
	AV	6,067,651	5/23/00	Rohrbaugh et al.	714	738	
	AW	6,079,037	6/20/00	Beffa et al.	714	720	
	AY						

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500426.02	APPLICATION NO. Not yet assigned
		APPLICANT(S) Brent Keeth	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not yet assigned

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	BA	0 283 906 A1	9/28/88	EP				X
	BB	0 828 252 A2	3/11/98	EP			X	
	BC	0 840 328 A2	5/6/98	EP			X	

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	BD		Descriptive literature entitled,"400MHz SLDRAM, 4Mx16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United States, pp. 1-22
	BE		"Draft Standards for a High-Speed Memory Interface (SyncLink)," Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-55.
	BF		Ishibashi, K. *et al.*, "A 6-ns 4-Mb CMOS SRAM with Offset-Voltage-Insensitive Current Sense Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, April 1995, pp. 480-486.
	BG		Kuroda, T. *et al.*, "Automated Bias Control (ABC) Circuit for High-Performance VLSI's," IEEE Journal of Solid-State Circuits, Vol. 27, No. 4, April 1992, pp. 641-648.
	BH		Nagai, T. et al., "A 17-ns 4-Mb CMOS DRAM," IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1538-1543
	BI		Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture," IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1493-1497
	BJ		Taguchi M. et al., "A 40ns 64Mb DRAM with Current-Sensing Data-Bus Amplifier," ISSCC Digest of Technical Papers, 1991, TAM 6.5.
	BK		
	BL		

EXAMINER	DATE CONSIDERED

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